





Now in Marathahalli!

We are thrilled to announce the opening of our new branch in Marathahalli, Bengaluru – your go-to destination for top-notch VLSI training and career development!



Courses We Offer

- Analog Design
- Analog Layout
- Design Verification
- RTL Design
- **FPGA**
- Physical Design
- **DFT**

Contact Us





Who Can Enroll?

- Engineering graduates
- Working professionals
- Final-year students

Why Choose Us?

- Expert Trainers
- Practical Labs
- Placement Support
- Flexible Timings





ASIC/IP DV TRAINING SYLLABUS

- DIGITAL ELECTRONICS & VERILOG
- VERILOG DESIGN AND VERIFICATION PROJECTS (TLC,1 PORT RAM-ROM,FIFO (SYNC,ASYNC),ELEVATOR FSM'S-4 TYPES)
- SV & SV PROJECT (RISC BASED MIPS PROCESSOR)
- UVM
- UVM PROJECTS (APB3 UVM VIP DEVELOPMENT, AXI3 DESIGN VERIFICATION, ETHERNET MAC 10G DESIGN VERIFICATION-VERIFICATION CODES ONLY WILL BE EXPLAINED)
- LINUX FOR DV
- SCRIPTING FOR DV
- TOOLS: MODELSIM, QUESTASIM, EDA PLAYGROUND, GVIM => IN
 FUTURE, WE MAY PROVIDE NEW ADVANCED TOOLS
- INTERVIEW GUIDANCE AND RESUME PREPARATION
- PRACTICE(PRESENTATION) SESSIONS TO IMPROVE
 PRESENTATION SKILLS, COMMUNICATION SKILLS, ENGLISH
- ASSIGNMENTS DAILY, EXAMS WEEKLY, MOCK INTERVIEWS
 MONTLY
- AFTER TRAINER SESSION, THERE WILL BE A MENTOR SESSION FOR PRACTICE, LAB AND FOR DOUBTS CLARIFICATION
- GUEST LECTURES (TECHNICAL AND FOR INTERVIEW PRACTICE)

 BY SENIOR INDUSTRY PROFESSIONALS

TRAINING EXCELLENCE ASSURED

- NOTE -1: AFTER COMPLETION OF ABOVE

 SYLLABUS, PLACEMENT PROCESS WILL START, WHILE

 APPLYING TO JOBS STUDENTS WILL LEARN

 PCIE/DDR/I3C(ANYONE/SOME/ALL)-VERIFICATION

 CODING AND/OR THEORY ONLY
- NOTE-2: OUR SYLLABUS WILL GIVE YOU KNOWLEDGE
 LEVEL OF 3+ YEARS EXPERIENCE
- NOTE-3: MAIN TRAINER(DEV), OF COURSE WE HAVE A
 TEAM OF 10+ TRAINERS AND 10+ MENTORS
- NOTE-4: AS PER INDUSTRY REQUIREMENT, WE UPDATE
 THE SYLLABUS
- NOTE -5: GIVING BEST TRAINING ACCORDING TO INDUSTRY STANDARD AND FACILITATING INTERVIEWS IS OUR RESPONSIBILITY THEN PROPER UTILIZATION OF TRAINING AND PERFORMING GOOD IN JOB INTERVIEWS IS THE STUDENT RESPONSIBILITY
- NOTE-6: RECORDINGS/MATERIALS WILL BE PROVIDED FOR E-LEARNING(FOR COURSE DURATION) & FOR ONLINE-OFFLINE ALSO(WITH LIMITED DAYS ACCESS ONLY).
- NOTE-7: COURSE COMPLETION CERTIFICATE PROVIDED

 BASED ON OVERALL COURSE PERFORMANCE

FEE:

RS. 50000(OFFLINE),

RS. 42000(ONLINE/E-LEARNING)
INCLUDING TAXES AND WITH
PLACEMENT SUPPORT.



ONLINE,E- LEARNING AND OFFLINE
(BANGALORE-MARATHAHALLI & HYDERABAD-SR NAGAR)
FOR PLACEMENTS



Contact Us

+91 99455 05962

FOR COURSE DETAILS





SYLLABUS

- DIGITAL ELECTRONICS
- FPGA BASED VERILOG CODING
- SVBASICS
- FPGA FUNDAMENTALS
- FPGA TOOLS,BOARDS: VIVADO,SPARTAN,ARTIX,ZYNQ,CIRCUIT

 VERSE,DOCKLIGHT => IN FUTURE,WE MAY PROVIDE CYCLONE

 BOARDS AND RELATED TOOLS
- FPGA EXPERIMENTS (COMBINATIONAL, SEQUENTIAL CIRCUITS)
- FPGA MINI PROJECTS (RTC, PWM, TLC, LCD, SEVEN SEGMENT DISPLAY, LDR, TEMPARATURE SENSOR, STOP WATCH/TIMER, ELEVATOR FSM'S-4 TYPES ETC)
- FPGA MAJOR PROJECTS (PLL, VGA, CORDIC IP, BROM IP, BRAM IP, XADC IP, FIFO IP, DMA-AXI IP, GPIO IP, SERIAL PROTOCOLS-UART, I2C, SPI)
- HLS(HIGH LEVEL SYNTHESIS)
- INTERVIEW GUIDANCE AND RESUME PREPARATION
- PRACTICE(PRESENTATION) SESSIONS TO IMPROVE PRESENTATION SKILLS, COMMUNICATION SKILLS, ENGLISH
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RS.40000(ONLINE/E-LEARNING)

INCLUDING TAXES WITH

PLACEMENT SUPPORT.

COURSE MODES:

ONLINE,E- LEARNING AND OFFLINE
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FOR PLACEMENTS



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FOR COURSE DETAILS





VLSI RTL COURSE SYLLABUS

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- SV BASICS AND SOME SV BASED DESIGN CODES
- MAIN DESIGN PROJECTS (APB3-AXI3-ETHERNET MAC 10G-PCIE ETC)
- TOOLS: MODELSIM, QUESTASIM, EDA

 PLAYGROUND, GVIM, CADENCE JASPER GOLD FOR FORMAL

 VERIFICATION & LEC, SPYGLASS FOR LINT, FOR SYNTHESIS
 CADENCE GENUS/SYNOPSYS-DC/FC ETC
- FPGA FUNDAMENTALS, VIVADO TOOL, SPARTAN FPGA ETC
- RTL CONCEPTS (RTL INTEGRATION-SYNTHESIS, LEC, LINTING, CDC ETC)
- INTERVIEW GUIDANCE AND RESUME PREPARATION
- PRACTICE(PRESENTATION) SESSIONS TO IMPROVE PRESENTATION SKILLS, COMMUNICATION SKILLS, ENGLISH
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FOR COURSE DETAILS



Trainee Engineers TESTINONIAL









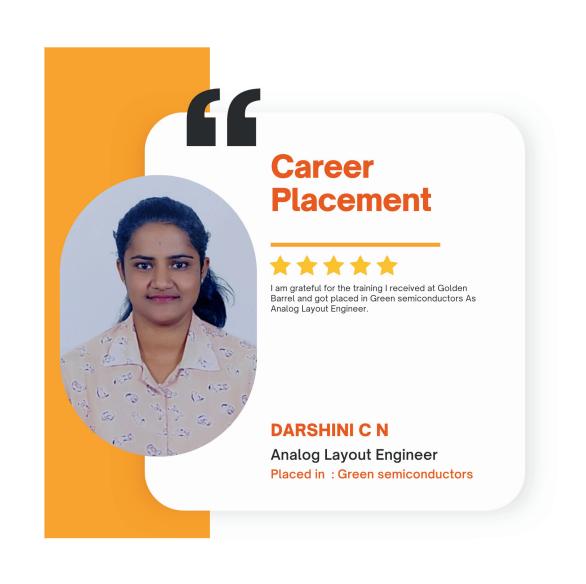




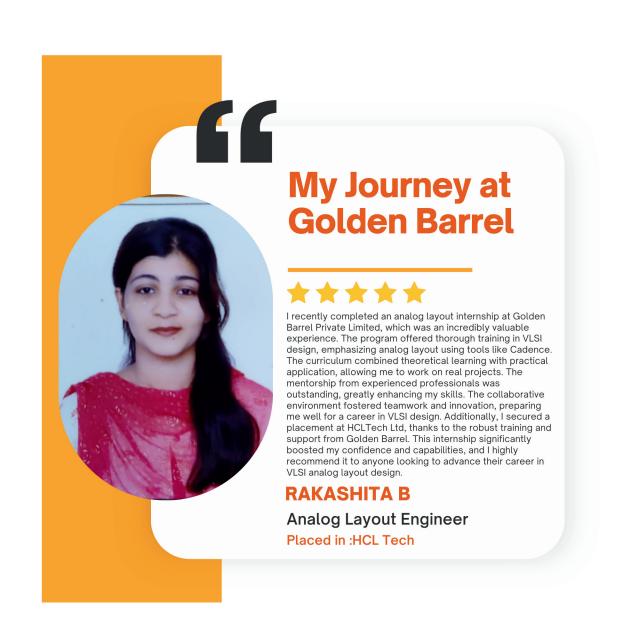


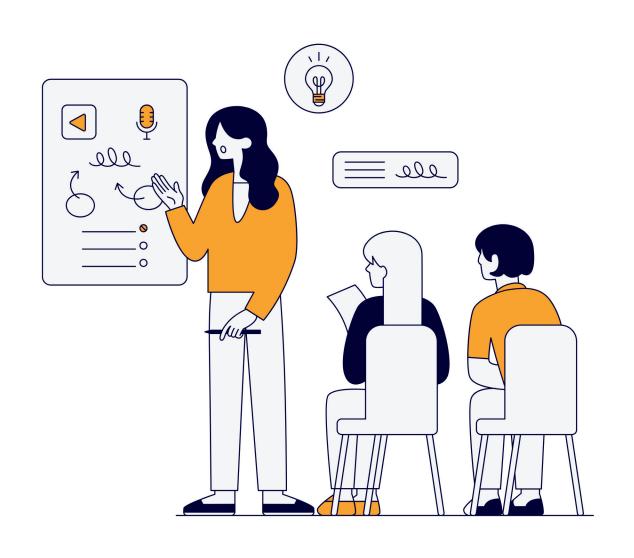












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CONTACT US

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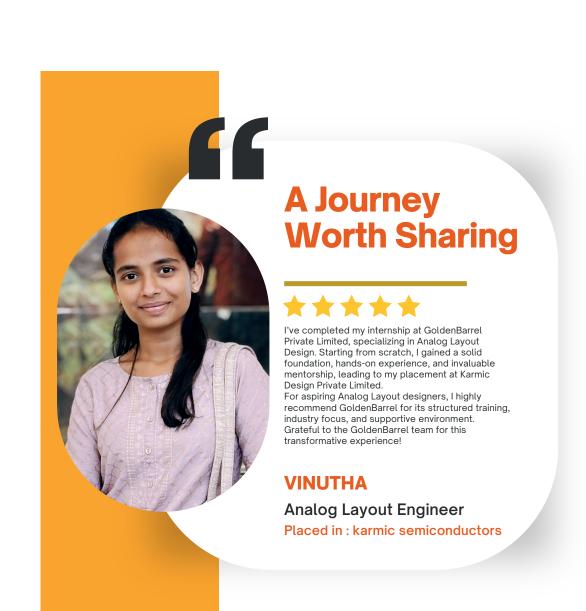
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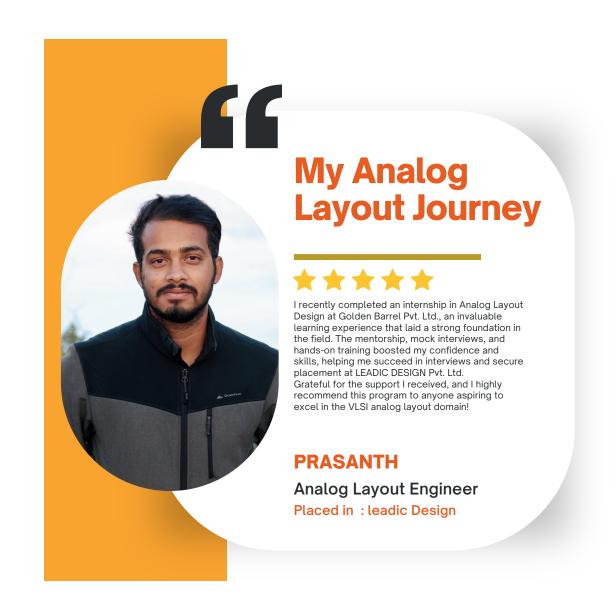
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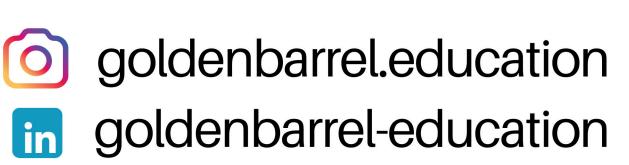
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